Designing High-Speed Transceiver Links with Confidence using Arria 10 FGPAs

Arria 10 FPGA and SoC Design Seminars 2013
Agenda

- Overview of Arria 10 Transceivers
- Designing High Speed Links - Best Practices
  - Material considerations
  - PCB Stack-up design considerations
  - High Speed Signal Integrity
- Driving high speed links with Arria 10 Transceivers
  - Equalization Schemes in Arria 10
  - On-Die Instrumentation
**Arria 10 Transceiver Overview**

- **Wide Range of Data Rates**
  - 611 Mbps – 28.1 Gbps (Native)
  - Down to 125 Mbps (Oversampling)

- **Increased Transceiver Density**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Arria 10</th>
<th>Stratix V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transceiver Count</td>
<td>Up to 96</td>
<td>Up to 66</td>
</tr>
<tr>
<td>Max Data Rate (Select Ch)</td>
<td>28.1 Gbps</td>
<td>28.1 Gbps</td>
</tr>
<tr>
<td>Max 28G Channels</td>
<td>16</td>
<td>4</td>
</tr>
<tr>
<td>Max Data Rate (All Ch)</td>
<td>17.4 Gbps</td>
<td>14.1 Gbps</td>
</tr>
<tr>
<td>Max Backplane Data Rate</td>
<td>17.4 Gbps</td>
<td>12.5 Gbps</td>
</tr>
</tbody>
</table>

*40% Greater Transceiver Port Density*
Arria 10 Transceiver Overview

- Support for a wide range of protocols, data rates, and applications
- Integrated protocol hard IP blocks
- Low jitter programmable clock sources
- Flexible clock distribution networks
- Gearbox for configurable interface widths
- Advanced adaptive equalization

Hard IP for:
- PCIe
- Ethernet
- 10GBASE-KR
- Interlaken
- More
## Arria 10 GX/GT Transceiver Support Targets

<table>
<thead>
<tr>
<th>Feature</th>
<th>Arria 10 GX/GT</th>
<th>Stratix V GS/GX/GT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Transceiver Count</td>
<td>96 @ 17.4 Gbps</td>
<td>66 @ 14.1 Gbps</td>
</tr>
<tr>
<td></td>
<td>16 @ 28.1 Gbps</td>
<td>4 @ 28.1 Gbps</td>
</tr>
<tr>
<td>Data Rate</td>
<td>28.1 Gbps chip-to-optical module</td>
<td>28.1 Gbps chip-to-optical module</td>
</tr>
<tr>
<td></td>
<td>17.4 Gbps chip-to-chip</td>
<td>14.1 Gbps chip-to-chip</td>
</tr>
<tr>
<td></td>
<td>17.4 Gbps backplane</td>
<td>12.5 Gbps backplane</td>
</tr>
<tr>
<td>Transmit Pre-emphasis</td>
<td>5-tap</td>
<td>4-tap</td>
</tr>
<tr>
<td>Adaptive CTLE (Continuous Time</td>
<td>Dual-Mode CTLE</td>
<td>High Gain CTLE</td>
</tr>
<tr>
<td>Linear Equalizer)</td>
<td>High Gain Mode</td>
<td></td>
</tr>
<tr>
<td></td>
<td>High Data Rate Mode</td>
<td></td>
</tr>
<tr>
<td>Adaptive DFE (Decision Feedback</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equalizer)</td>
<td>7-tap (fixed)</td>
<td>5-tap (fixed only)</td>
</tr>
<tr>
<td></td>
<td>4-tap (floating)</td>
<td></td>
</tr>
<tr>
<td>Hard Forward Error Correction (FEC)</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Total System Equalization</td>
<td>&gt; 30 dB (not Including FEC)</td>
<td>Up to 25 dB</td>
</tr>
<tr>
<td>Capability</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Performance Boost Across the Board**

*Bold: Denotes significant upgrade from Stratix V*
High Speed Serial Transceiver Link Design

- High Speed PCB Design for 10 Gbps to 28 Gbps
  - Materials Consideration
  - Trace Design
  - Via Design
  - Channel Breakouts
  - AC cap optimization
  - Connectors
  - Other factors
Transceiver Applications
Arria 10 High Speed Equalization
Arria 10 TX Block Architecture

Low Jitter Clock Sources

Clock Sources
- ATX PLL
- CMU PLL
- fPLL

Simplified Clock Distribution

Voltage Mode Output Driver

5-tap Transmit Pre-Emphasis

Flexible Serializer Bus Width

Clock Distribution

Ser

TX Pre-Emphasis

Clock Buffers

TX Driver

Clock Sources

Low Jitter Clock Sources

Voltage Mode Output Driver

5-tap Transmit Pre-Emphasis

Flexible Serializer Bus Width

Feature | Capability | Benefit
---|---|---
ATX PLL | Lowest jitter clock source | Continuous data rate control to 28.1 Gbps
Clock Distribution | Multiple clock distribution paths | Maximize channel utilization
Pre-Emphasis | 5-tap control | Equalization for backplane and optical
TX Driver | Voltage mode output driver | 50% reduced power
**Arria 10 RX Block Architecture**

- **Dual-Mode Continuous Time Linear Equalizer (CTLE)**
- **Variable Gain Amplifier (VGA)**
  - **VGA**
  - **Σ**
  - **DFE**
  - **EyeQ**
- **Digital Adaptive Parametric Tuning**
- **High Resolution Eye Measurement**
- **All new Floating Tap Decision Feedback Equalizer**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Capability</th>
<th>Benefit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual Mode CTLE</td>
<td>High Gain and High Data Rate Modes</td>
<td>28G with noise reduction</td>
</tr>
<tr>
<td>VGA</td>
<td>Adaptive Variable Gain</td>
<td>Wide dynamic range</td>
</tr>
<tr>
<td>DFE</td>
<td>7-fixed and 4-floating taps</td>
<td>ISI compensation and noise suppression</td>
</tr>
<tr>
<td>ADAPT</td>
<td>Automatic Digital Parametric Adaptation</td>
<td>Simplified adaptive equalization support</td>
</tr>
<tr>
<td>EyeQ</td>
<td>4X Resolution</td>
<td>On chip eye monitoring</td>
</tr>
</tbody>
</table>
Dual Mode Continuous Time Linear Equalizer (CTLE)

- **High Gain Mode**
  - High and Low Bandwidth selection
    - Peaking at 6.5 Gbps, 12.5 Gbps
    - 4-stages
    - 15 dB programmable AC gain
  - Usage: High Loss Systems up to 16 Gbps

- **High Data Rate Mode**
  - Broadband Gain
    - Programmable Peaking Frequency
  - Usage: 28 Gbps and/or High Crosstalk Systems
    - For data rates > 12.5 Gbps

<table>
<thead>
<tr>
<th>Modes</th>
<th>Arria 10</th>
<th>Stratix V</th>
<th>Arria V</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Gain Mode</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>High Data Rate Mode</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>

*Not to scale*
Variable Gain Amplifier (VGA)

- **Variable Gain Amplifier**
  - Adaptive DC Gain Control

- **Match input signal amplitude to DFE dynamic range**
  - Improves Gain of DFE
  - Automatic VGA Adaptation

- **Example**

![Diagram showing the process of variable gain amplifier and its effect on signal amplitude]

1000 mV

100 mV

Optimal DFE Dynamic Range

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Decision Feedback Equalizer (DFE)

- **DFE Use Cases**
  - Equalize post-cursor intersymbol interference (ISI)
  - Improve signal-noise-ratio (SNR) / eye margin
  - Mitigate Effects of Crosstalk Noise

- **New Floating Tap DFE Architecture**
  - 7-taps fixed
  - 4-taps floating

- **New Adaptation Engine**
  - Master Digital Adaptive Parametric Tuning Engine (ADAPT)
  - Continuous DFE Tap Weight Adaptation

<table>
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<tr>
<th>Feature</th>
<th>Arria 10</th>
<th>Stratix V</th>
</tr>
</thead>
<tbody>
<tr>
<td>DFE Taps</td>
<td>Fixed and Floating</td>
<td>Fixed</td>
</tr>
<tr>
<td>Adaptation</td>
<td>Continuous and Triggered</td>
<td>Triggered</td>
</tr>
</tbody>
</table>
Altera Digital Adaptive Parametric Tuning (ADAPT)

- **Automatic Adaptation Engine**
  - Master sequencing and coordination block for multiple adaptation loops

- **Fully Digital Adaptation Implementation**

- **Initialize RX parameters on link bring-up**

- **Dynamically adjust RX parameters during operation**

<table>
<thead>
<tr>
<th>Block</th>
<th>Auto Adaptive Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTLE</td>
<td>AC Gain</td>
</tr>
<tr>
<td>VGA</td>
<td>Signal Amplitude (DC Gain)</td>
</tr>
<tr>
<td>DFE</td>
<td>DFE Tap Weights</td>
</tr>
<tr>
<td>Threshold</td>
<td>CDR Bit Slicer Threshold</td>
</tr>
</tbody>
</table>
EyeQ Eye Viewer Tool

- View receiver signal margin and link BER
- Vertical and horizontal reconstruction of eye
  - 128 Vertical Steps, 64 Horizontal Steps
    - 4X resolution compared to Stratix V
- View eye on live traffic
- One EyeQ block in each channel
  - Accessible simultaneously
**Equalization Use Cases**

- **CTLE, VGA, and DFE work together to equalize channel**
  - Master Digital Adaptive Parametric Tuning Engine for adaptive blocks

<table>
<thead>
<tr>
<th>Channel Conditions</th>
<th>TX Pre-Emphasis</th>
<th>CTLE</th>
<th>VGA</th>
<th>DFE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip-to-Chip</td>
<td>Enable</td>
<td>High Gain Mode</td>
<td>Disable</td>
<td>Disable</td>
</tr>
<tr>
<td>Chip-to-CFP2 Optical Module</td>
<td>Enable</td>
<td>High Data Rate Mode</td>
<td>Disable</td>
<td>Disable</td>
</tr>
<tr>
<td>High Loss Backplane</td>
<td>Enable</td>
<td>High Gain Mode</td>
<td>Enable</td>
<td>Fixed Taps</td>
</tr>
<tr>
<td>Reflective Channel or Backplane (i.e. from via stubs)</td>
<td>Disable</td>
<td>High Data Rate Mode</td>
<td>Enable</td>
<td>Fixed and Floating Taps</td>
</tr>
<tr>
<td>High Crosstalk Channel</td>
<td>Disable</td>
<td>Disable</td>
<td>Enable</td>
<td>Fixed Taps</td>
</tr>
</tbody>
</table>
Learn More

Technical Application Notes
- AN528: PCB Material Selection and Fiber Weave Effect on High-Speed Routing
- AN613: PCB Stackup Design Considerations for Altera FPGAs
- AN672: Transceiver Link Design Guidelines for High-Gbps Data Rate Transmission
- AN574: Power Delivery Network (PDN) Design Methodology
- AN529: Via Optimization Techniques for High-Speed Channel Design
- AN530: Optimizing Impedance Discontinuity Caused by Surface Mount Pads
- Wiki: Modeling Copper Surface Roughness for Multi-gigabit Channel Designs

Webpages
- Arria 10 Product Webpage: Arria 10 FPGAs
- Altera Board Design Portal: altera.com/board
Thank You